38. A semiconductor device according to claim 37 wherein said first type of stress is tensile stress, said second type of stress is compressive stress and said layer of conductive interconnectors is sandwiched between two insulating layers having compressive stress.

39. A semiconductor device according to claim 37, wherein said interconnectors are aluminum.

40. A semiconductor device according to claim 37 having an overall stress for the whole of the plurality of insulating layers less than 3 X 10^5 ~~dyne/cm~~ dyne/cm^2.

REMARKS

The new claims are directed to the structure shown in Fig. 10a of applicants' drawings. As described at pages 30-32 of applicants' Substitute Specification, layers 34 are formed by plasma CVD and layers 35 are formed by thermal CVD. Fig. 10a represents the "third embodiment" described in applicants' specification and, as noted at the bottom of page 29 of the Substitute Specification, the insulating layers of the "third embodiment" were formed in the same manner that the insulating layers of Sample S1 were formed in the first embodiment. As described at pages 12 and 13 of applicants' specification, the plasma CVD films of Sample S1 were formed with compressive stress

whereas the thermal CVD films were formed with tensile stress. Thus, the interconnectors 33 shown in Fig. 10a are each sandwiched between insulating layers having the same type stress. In this manner, the stress between the layers sandwiching the wiring is minimized and the wiring is protected against breakage.

In contradistinction, in Itoh et al, as shown in Fig. 5(e), wiring 31 is formed between insulating film 412 having compressive stress and insulating film 421 having tensile stress.

Respectfully submitted,

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